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FORM PTO-1390 (REV 11-2000) DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NO
		851663.433USPC
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S APPLICATION NO (If known, see37 CFR 1 5) Unknown 10/088976
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/SG00/00108	**26 July 2000 (26.07.00)**	**N/A**

TITLE OF INVENTION

A THERMAL SENSOR CIRCUIT

APPLICANT(S) FOR DO/EO/US

RAVISHANKER, Krishnamoorthy

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 – 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4)
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items of information:

U.S. APPLICATION NO (If known, see 37 CFR 1 5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
Unknown 10/088976	**PCT/SG00/00108**	**851663.433USPC**

21. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

	CALCULATIONS PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00	
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)..... $710.00	
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =				$890.00
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$130.00
Claims	Number Filed	Number Extra	Rate	
Total Claims	19 - 20 =	0	x $ 18.00	$0.00
Independent Claims	3 - 3 =	0	x $ 84.00	$0.00
Multiple dependent claim(s) (if applicable)			+ $280.00	$0.00
TOTAL OF ABOVE CALCULATIONS =				$1,020.00
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$.00
SUBTOTAL =				$.00
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$.00
TOTAL NATIONAL FEE =				$.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$.00
TOTAL FEES ENCLOSED =				**$1,020.00**
				Amount to be refunded
				charged

a. ☒ A check in the amount of $1,020.00 cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. in the amount of $_ to cover the above fees. A duplicate copy of this sheet is enclosed.

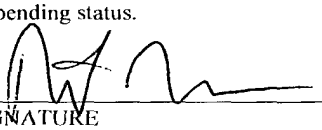
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **19-1090**. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Robert Iannucci, Esq.
Seed Intellectual Property Law Group PLLC
701 5th Avenue, Suite 6300
Seattle, WA 98104-7092
United States of America
(206) 622-4900



SIGNATURE

Robert Iannucci
NAME

33,514
REGISTRATION NUMBER

PATENT COOPERATION TREATY

Int'l Application No.	:	PCT/SG00/00108
Int'l Filing Date	:	26 July 2000
U.S. Application No.	:	Not yet known
Inventors	:	RAVISHANKER, Krishnamoorthy
Title	:	A THERMAL SENSOR UNIT
Docket No.	:	851663.433USPC
Date	:	26 March 2002

Box PCT
Assistant Commissioner for Patents
Washington, DC 20231-0001

PRELIMINARY AMENDMENT

Sir:

Applicants respectfully request entry of preliminary amendments in the above-identified United States National Phase patent application. Please amend the claims as follows:

In the Claims:

Please amend Claims 5 and 6 as follows:

5. (Amended) The thermal sensor circuit of claim 3 wherein each of the first to sixth BJTs is an n-p-n transistor.

6. (Amended) The thermal sensor circuit of claim 3 wherein the current gain is given by:

$$\frac{I2}{I1} = \frac{\beta^2 + (3+N)\beta}{\beta^2 + \beta + (2+N)}$$

where:

$I1$ is the first current input;

$I2$ is the second current input; and

β is the common-emitter current gain of each of the first to sixth BJTs.

Please enter the following new claims 8-19.

8. A thermal sensor circuit for sensing the temperature of an integrated circuit chip, the thermal sensor circuit comprising:

a sensing device that produces a sensed voltage corresponding to the temperature of the integrated circuit chip;

a first current mirror having first and second mirror legs respectively carrying first and second mirror currents that are directly proportional to each other, the first mirror leg being in series with the sensing device; and

a compensation circuit that includes:

an input that receives an input current;

a first transistor coupled between the input and a first supply voltage reference and having a control terminal;

a second transistor coupled between the second mirror leg and the first supply reference and having a control terminal coupled to the control terminal of the first transistor; and

a third transistor coupled between a second supply voltage reference and the first supply voltage reference and having a control terminal coupled to the control terminals of the first and second transistors.

9. The thermal sensor circuit of claim 8 wherein the compensation circuit further includes a fourth transistor coupled between the second mirror leg and the control terminals of the first, second, and third transistors, and having a control terminal coupled to the input of the compensation circuit.

10. The thermal sensor circuit of claim 9 wherein the first, second, third, and fourth transistors are bipolar transistors.

11. The thermal sensor circuit of claim 8, further comprising:

an output comparator having first and second inputs and an output, the first input being coupled to the sensing device to receive the sensed voltage;

a reference voltage circuit having an input and an output at which a reference voltage is produced, the output of the reference voltage circuit being coupled to the second input of the output comparator; and

a second current mirror having a first mirror leg coupled to the reference voltage circuit, and a second mirror leg coupled to the input of the compensation circuit to provide the input current.

12. The thermal sensor circuit of claim 11 wherein the second current mirror has a third mirror leg and the reference voltage circuit includes:

a fourth transistor coupled between the third leg of the second current mirror and the first supply voltage reference and having a control terminal corresponding to the output of the voltage reference circuit; and

a fifth transistor coupled between the first leg of the second current mirror and the first supply voltage reference and having a control terminal corresponding to the output of the voltage reference circuit.

13. The thermal sensor circuit of claim 12, wherein a ratio of an emitter area of the fifth transistor to an emitter area of the sixth transistor is M:1, where M>1.

14. The thermal sensor circuit of claim 11 wherein the first and second current mirrors are connected to the second supply voltage reference and include p-n-p bipolar transistors in their respective first and second mirror legs.

15. A thermal sensor circuit for sensing the temperature of an integrated circuit chip, the thermal sensor circuit comprising:

a sensing device that produces a sensed voltage corresponding to the temperature of the integrated circuit chip;

an output comparator having first and second inputs and an output, the first input being coupled to the sensing device to receive the sensed voltage;

a reference voltage circuit having a first input and an output at which a reference voltage is produced, the output of the reference voltage circuit being coupled to the second input of the output comparator;

a first current mirror having first and second outputs, the first output being coupled to the first input of the reference voltage circuit;

a second current mirror having first and second outputs, the first output being coupled to the sensing device; and

a compensation circuit having first and second inputs coupled respectively to the second outputs of the first and second current mirrors.

16. The thermal sensor circuit of claim 15 wherein the compensation circuit includes:

a first transistor coupled between the first input of the compensation circuit and a first supply voltage reference and having a control terminal;

a second transistor coupled between the second input of the compensation circuit and the first supply reference and having a control terminal coupled to the control terminal of the first transistor; and

a third transistor coupled between a second supply voltage reference and the first supply voltage reference and having a control terminal coupled to the control terminals of the first and second transistors.

17. The thermal sensor circuit of claim 16 wherein the compensation circuit further includes a fourth transistor coupled between the second input of the compensation circuit and the control terminals of the first, second, and third transistors, and having a control terminal coupled to the first input of the compensation circuit.

18. The thermal sensor circuit of claim 17 wherein the first, second, third, and fourth transistors are bipolar transistors.

19. The thermal sensor circuit of claim 15 wherein the first current mirror includes:

a first mirror leg coupled between a supply voltage and the first input of the compensation circuit;

a second mirror leg coupled between the supply voltage and the first input of the reference voltage circuit; and

a third mirror leg coupled between the supply voltage and a first input of the reference voltage circuit.

REMARKS

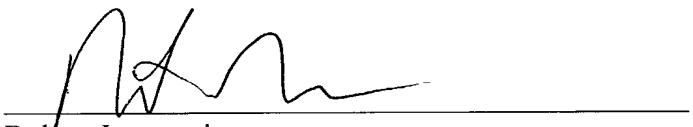
Claims 1-19 will be pending upon entry of the present amendment. Claims 5-6 are being amended. Calims 8-19 are being newly presented.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made**."

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Seed Intellectual Property Law Group PLLC



Robert Iannucci
Registration No. 33,514

RXI:km

Enclosure: Appendix

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
(206) 622-4900; Fax: (206) 682-6031

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 5-6 as follows.

5. (Amended) The thermal sensor circuit of claim 3 ~~or claim 4~~, wherein each of the first to sixth BJTs is an n-p-n transistor.

6. (Amended) The thermal sensor circuit of claim 3 ~~or claim 4~~, wherein the current gain is given by:

$$\frac{I2}{I1} = \frac{\beta^2 + (3+N)\beta}{\beta^2 + \beta + (2+N)}$$

where:

$I1$ is the first current input;

$I2$ is the second current input; and

β is the common-emitter current gain of each of the first to sixth BJTs.

A THERMAL SENSOR CIRCUIT

FIELD OF THE INVENTION

The present invention relates to thermal sensor circuits. In particular, the invention relates to thermal sensor circuits for sensing temperature-related characteristics of a semiconductor device.

BACKGROUND OF THE INVENTION

Integrated circuits (ICs) are generally manufactured on semiconductor substrates (also called wafers) by a process involving deposition. Other semiconductor materials are thermally driven into the substrate. Because of the small size of the ICs, numerous ICs are fabricated using a single dye on the same wafer. The ICs are then separated by cutting. Due to unpredictable variations in the manufacturing process from dye to dye, as well as from wafer to wafer, the characteristics of the individual ICs are not identical. By measuring the characteristics of the manufactured ICs, these variations can be found.

In order to sense the temperature of the IC, a thermal sensor circuit is formed on the chip carrying the IC. If the variations in the temperature sensing characteristics of the sensor circuit are not within an acceptable range, the IC must be discarded as being defective, resulting in a lower IC manufacturing yield. It is therefore desirable to provide compensation for the manufacturing process variations so that the ICs need not be discarded.

The circuit components of the thermal sensor circuit on each IC chip will generally be sufficiently proximate to each other that they will all be affected by the process variations to a similar extent.

An example of a conventional temperature sensor circuit is shown in Figure 1. The temperature is sensed by comparing the linearly varying voltage at V_{sense} with the (ideally) fixed reference voltage V_{ref}. For example, if V_{sense} is 0 volts at 20 degrees Celsius and 1 volt

at 120 degrees, for every 10 degrees V_{sense} increases by 0.1 volts. If it is desired to detect when the temperature reaches 100 $_{degrees,}$ V_{ref} should be set to 0.8 volts. When V_{sense} is less than 0.8 volts, the temperature will be below 100 degrees and the comparator output will be low. When V_{sense} is greater than 0.8 volts, the temperature will be greater 100 degrees and the comparator output will be high. In order to accurately sense whether the temperature of the IC has passed a particular threshold temperature, V_{ref} must not vary with temperature. Otherwise this will give a spurious result as to the sensed voltage at the output of the comparator. However, due to IC manufacturing process variations, V_{ref} will sometimes vary with temperature.

In order for all the manufactured ICs to meet the required parameters, the process variations need to be taken into account during the design stage of the ICs. The circuits sensitivity to these process parameters must be minimized to get minimal difference in the performance of the circuit from IC to IC.

Transistors Q1 and Q2 are used to generate a voltage across the resistor R1 which is independent of any process variation. This voltage is effectively a property of the Silicon of the transistors and is therefore accurately reproducible. The voltage across the resistor R1 is given by the difference of the base-emitter potentials of transistors Q1 and Q2,

$$V_{be1} - V_{be2} = k \cdot T \cdot \ln(M)$$

where k is Boltzmann's constant, T is absolute temperature and M is the ratio (M:1, for $M > 1$) of the emitter areas of Q2 to Q1. The temperature sense voltage V_{sense} is measured over the temperature sensing resistor R3 and is given by,

$$V_{sense} = \frac{R3}{R1} \cdot k \cdot T \cdot \ln(M)$$

It is clear from the equation above that the V_{sense} is not affected by variations in the process,

since the process dependent components in the equation, resistors R3 and R1, appear as a ratio and will generally be affected by the process variations to the same extent. The "current mirror 1" circuit shown in Figure 1 is modelled as an ideal p-n-p current mirror for simplicity of explanation.

A reference "bandgap" voltage is obtained at the base of Q1 and Q2, such that the value is almost constant over temperature and is given by,

$$V_{ref} = V_{be1} + \frac{R2}{R1} \cdot k \cdot T \cdot \ln(M)$$

As the temperature varying term of the above equation is small relative to the base-emitter voltage of transistor Q1, V_{ref} changes as V_{be1} changes due to process variations.

Figure 3a illustrates the relationships of V_{sense} and V_{ref} over varying voltage and temperature. As can be seen from the plot of Figure 3a, the normal level of Vref will be crossed by the linearly varying Vsense measurement at the desired temperature level, T0. When the process variations have resulted in changed characteristics of the sensing circuit, this will have the effect of changing the level of Vref so that, for characteristics corresponding to the 'process minimum', Vref will be higher and will be crossed by Vsense at a higher temperature, T2, and for characteristics corresponding to the 'process maximum', Vref will be lower and will be crossed by Vsense at a lower temperature, T1. Temperatures T1 and T2 are spurious results, which, if the temperature differential between these two values is large, can cause an unacceptably high number of occurrences of spurious high temperature alert signals for the IC.

Figure 3b shows the output of the comparator corresponding to the spurious temperature detections at temperatures T1 and T2 as shown in Figure 3a.

It is therefore desirable to reduce the temperature difference (ie. T2 - T1) over which spurious detections occur for thermal sensing circuits in order to reduce the number of occurrences of

spurious high temperature alert signals for the IC.

SUMMARY OF THE INVENTION

The present invention provides a thermal sensor circuit for sensing the temperature of an integrated circuit chip, the thermal sensor circuit including:

an output comparator for comparing a reference voltage, V_{ref}, with a sensed voltage, V_{sense}, the sensed voltage being measured from a sensing device;

a first circuit to which a reference voltage line is connected to measure V_{ref};

a first current mirror providing a first current input to the first circuit and to a compensation circuit;

a second current mirror providing a second current input to the compensation circuit and to the sensing device; and wherein

the compensation circuit provides a current gain, defined as the ratio of the second current input to the first current input, for compensating for variations in V_{ref} due to variations of the characteristics of the thermal sensing circuit arising from manufacture by adjusting the second current input in dependence on the variations of the characteristics to thereby vary V_{sense} with V_{ref}.

Preferably, the compensation circuit includes first, second, third and fourth bipolar junction transistors (BJTs) wherein:

the first BJT has a collector terminal connected to the first current input of the first current mirror, a base terminal connected to a common base connection and an emitter terminal connected to ground;

the second BJT has a collector terminal connected to the second current input of the second current mirror, a base terminal connected to the common base connection and an emitter terminal connected to ground;

the third BJT has a collector terminal connected to the second current input, a base terminal connected the first current input and an emitter connected to the common base connection;

the fourth BJT has a collector terminal connected to a voltage supply of the thermal

sensor circuit, a base terminal connected to the common base connection and an emitter terminal connected to ground; and

the ratio of emitter area of the fourth BJT to the emitter areas of the first, second and third BJTs is N : 1, where $N > 0$.

Preferably, the first circuit includes fifth and sixth BJTs, wherein:

the fifth BJT has a collector terminal connected to the first current input, a base terminal connected to the reference voltage line and an emitter terminal connected to an output point of the first circuit via a first resistor;

the sixth BJT has a collector terminal connected to the first current input, a base terminal connected to the reference voltage line and an emitter connected to the output point of the first circuit;

the output point of the first circuit is connected to ground via a second resistor.

Preferably, the ratio of emitter area of the fifth BJT to the emitter area of the sixth BJT is M:1, where $M > 1$. Preferably, each of the first to sixth BJTs is an n-p-n transistor.

Preferably, the current gain is given by:

$$\frac{I2}{I1} = \frac{\beta^2 + (3+N)\beta}{\beta^2 + \beta + (2+N)}$$

where:

$I1$ is the first current input;

$I2$ is the second current input; and

β is the common-emitter current gain of each of the first to sixth BJTs.

Preferably, the first and second current mirrors are connected to the voltage supply of the thermal sensor circuit and use p-n-p BJTs to supply the first and second current inputs, respectively.

Advantageously, the thermal sensor circuit provides a compensation function which reduces

the temperature range over which spurious temperature detection signals are sent by the comparator by providing a compensation circuit which provides current gain to adjust V_{sense} according to the degree of process variations effected by the manufacturing process of the IC on the thermal sensing circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram of a known temperature sensing circuit;

Figure 2 is a circuit diagram of a known current mirror circuit;

Figure 3a is a graph of voltage versus temperature, showing the relationship between the sensed voltage and the reference voltage of the temperature sensing circuit of Figure 1;

Figure 3b is a plot of the output of the comparator of the temperature sensing circuit of Figure 1 corresponding to the graph of Figure 3a;

Figure 4 is a circuit diagram of a modified current mirror circuit employed in an embodiment of the invention;

Figure 5 is a circuit diagram of a temperature sensing circuit according to an embodiment of the invention;

Figure 6a is a graph of voltage versus temperature, showing the relationship between the sensed voltage and the reference voltage of the temperature sensing circuit of Figure 5;

Figure 6b is a plot of the output of the comparator of the temperature sensing circuit of Figure 5 corresponding to the graph of Figure 6a;

Figure 7 is a comparative plot of current gain versus process variation.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A typical n-p-n current mirror circuit is shown in Figure 2, the current gain (I2/I1) of which is given by,

$$Gain = \frac{I2}{I1} = \frac{\beta^2 + \beta}{\beta^2 + \beta + 2}$$

where β is the common-emitter current gain of a BJT. Generally, a process minimum corresponds to a smaller β, and is called a process minimum because the circuits tend to operate more slowly. Similarly, a process maximum corresponds to a larger β, where the circuits tend to operate faster. For smaller values of β, the current gain is less than 1. As β increases, the gain approaches 1.

A compensation circuit 10 is shown in Figure 4, similar to that shown in Figure 2 except for a few important differences. Compensation circuit 10 includes an additional transistor Qd, the base terminal of which is connected to the common base connection of current mirror transistors Qa and Qb and the collector terminal of which is connected to the supply voltage, Vdd, of the thermal sensor circuit. The emitter terminal of Qd is connected to ground 14, in common with the emitter terminals of Qa and Qb. The emitter area of Qd is larger than the emitter areas of Qa, Qb and Qc by a ratio of N:1, where $N \geq 0$. N will usually be equal to or larger than 1 but may effectively be zero by providing an open circuit in place of Qd. Also in contrast to Figure 2, instead of the collector of transistor Qc being connected to the supply voltage Vdd, it is connected in parallel with the collector of Qb. The gain of the compensation circuit of Figure 4 is given by:

$$\frac{I2}{I1} = \frac{\beta^2 + (3+N)\beta}{\beta^2 + \beta + (2+N)}$$

Figure 5 shows the compensation circuit 10 of Figure 4 in use in a thermal sensing circuit 2.

The compensation circuit 10 is placed in combination with first and second current mirrors 6, 7, a bandgap reference circuit 8 and a comparator 4. The bandgap reference circuit 8 and the comparator 4 operate in a similar manner to that of the thermal sensor circuit of Figure 1. Transistors Q1, Q2 of the reference circuit and Qa, Qb, Qc and Qd of the compensation circuit are all n-p-n transistors having similar characteristics (apart from the larger emitter areas of Q2 and Qd).

The relative sizes of resistors R1, R2 and R3 serve to define the levels of V_{ref} and V_{sense} and will be set according to the threshold temperature which it is desired to detect the passing of. Typically, R2 and R3 are of similar values while R1 is relatively much smaller.

The reference current I1 from the first current mirror 6 is given a current gain by the compensation circuit 10 to draw a compensated output current I2 from current mirror 7. The current I2 drawn through the compensation circuit must, by the nature of an ideal current mirror, be reflected through the other current supply line of the current mirror 7 which runs through thermal sensing resistor R3 to give a potential difference over R3 corresponding to V_{sense}. Thus, the compensation circuit 10 provides a current gain of I2 with respect to I1. The current gain provided (I2/I1) is more than the typical value when the process is minimum and less than the typical gain when the process is maximum.

Some sample gain values are calculated below:

Process minimum ⇒ small β; increased V_{ref}.
Process mean ⇒ typical β; normal V_{ref}.
Process maximum ⇒ larger β; decreased V_{ref}.

For the typical current mirror:
Small $\beta = 5$; $I2/I1 = 0.938 < 1$;
Typical $\beta = 20$; $I2/I1 = 0.995$.
Larger $\beta = 50$; $I2/I1 = 0.999 \approx 1$.

For the compensation circuit, with N=1:

Small $\beta = 5$; I2/I1 = 1.364> 1;

Typical $\beta = 20$; I2/I1 = 1.135.

Larger $\beta = 50$; I2/I1 = 1.058 ≈ 1.

The thermal sensor circuit 2 having the compensation circuit 10 therefore provides compensation for the process variations by providing a current gain to adjust the sensed voltage, V_{sense}, over thermal sensing resistor R3. The compensated V_{sense} is given by:

$$V_{sense\ (compensated)} = \frac{\beta^2 + (3+N)\beta}{\beta^2 + \beta + (2+N)} \cdot \frac{R3}{R1} \cdot k \cdot T \cdot \ln(M)$$

In an alternative embodiment of the invention, the current mirrors 6 and 7 may be implemented with n-p-n transistors and the reference and compensation circuits may be implemented with p-n-p transistors. This would necessitate a reversal of polarity for the terminals of the comparator 4 and would require changing the relative roles of the voltage supply and ground lines.

Figure 6a shows a plot (which is not to scale) of V_{ref} and V_{sense} versus temperature for the compensated thermal sensor circuit 2. It can be seen that V_{sense} is increased for process minimum scenarios and is decreased for process maximum scenarios. This compensation of V_{sense} reduces the temperature range over which spurious temperature measurements are recorded, leading to greater accuracy of the thermal sensor circuit, fewer ICs being discarded because of irredeemable process variations and a correspondingly higher IC manufacturing yield. Figure 6b shows the output of the comparator 4 corresponding to reduced band of spurious temperature detections at temperatures T1 and T2 as shown in Figure 6a.

Advantageously, by appropriately choosing the area of Qd, the current gain of the compensation circuit can be modified to effectively provide a 'DC shift' to the measured V_{sense} in order to track the variations in Vref due to process variations, thereby enabling an accurate sensing of the temperature independent of the process variations. The amount of variation in the current gain, and hence compensation of Vsense, can be adjusted by changing the emitter

area N of transistor Qd to suit a particular batch of IC chips.

Figure 7 shows the relationship between the current gain and the process variations for both the proposed compensation circuit (for N=0, 1 and 2) and an exemplary "typical mirror" circuit employed in place of the compensation circuit in Figure 5. The use of the "typical mirror" in place of the compensation circuit in Figure 5 is not believed to form part of the prior art but is used here for the purposes of comparison.

CLAIMS:

1. A thermal sensor circuit for sensing the temperature of an integrated circuit chip, the thermal sensor circuit including:

an output comparator for comparing a reference voltage, V_{ref}, with a sensed voltage, V_{sense}, the sensed voltage being measured from a sensing device;

a first circuit to which a reference voltage line is connected to measure V_{ref};

a first current mirror providing a first current input to the first circuit and to a compensation circuit;

a second current mirror providing a second current input to the compensation circuit and to the sensing device; and wherein

the compensation circuit provides a current gain, defined as the ratio of the second current input to the first current input, for compensating for variations in V_{ref} due to variations of the characteristics of the thermal sensing circuit arising from manufacture by adjusting the second current input in dependence on the variations of the characteristics to thereby vary V_{sense} with V_{ref}.

2. The thermal sensor circuit of claim 1, wherein the compensation circuit includes first, second, third and fourth bipolar junction transistors (BJTs) and wherein:

the first BJT has a collector terminal connected to the first current input of the first current mirror, a base terminal connected to a common base connection and an emitter terminal connected to ground;

the second BJT has a collector terminal connected to the second current input of the second current mirror, a base terminal connected to the common base connection and an emitter terminal connected to ground;

the third BJT has a collector terminal connected to the second current input, a base terminal connected the first current input and an emitter connected to the common base connection;

the fourth BJT has a collector terminal connected to a voltage supply of the thermal sensor circuit, a base terminal connected to the common base connection and an emitter terminal connected to ground; and

the ratio of emitter area of the fourth BJT to the emitter areas of the first, second and third BJTs is N : 1, where $N > 0$.

3. The thermal sensor circuit of claim 2, wherein the first circuit includes fifth and sixth BJTs, and wherein:

the fifth BJT has a collector terminal connected to the first current input, a base terminal connected to the reference voltage line and an emitter terminal connected to an output point of the first circuit via a first resistor;

the sixth BJT has a collector terminal connected to the first current input, a base terminal connected to the reference voltage line and an emitter connected to the output point of the first circuit; and

the output point of the first circuit is connected to ground via a second resistor.

4. The thermal sensor circuit of claim 3, wherein the ratio of emitter area of the fifth BJT to the emitter area of the sixth BJT is M : 1, where $M > 1$.

5. The thermal sensor circuit of claim 3 or claim 4, wherein each of the first to sixth BJTs is an n-p-n transistor.

6. The thermal sensor circuit of claim 3 or claim 4, wherein the current gain is given by:

$$\frac{I2}{I1} = \frac{\beta^2 + (3+N)\beta}{\beta^2 + \beta + (2+N)}$$

where:

$I1$ is the first current input;

$I2$ is the second current input; and

β is the common-emitter current gain of each of the first to sixth BJTs.

7. The thermal sensor circuit of claim 2, wherein the first and second current mirrors are connected to the voltage supply of the thermal sensor circuit and use p-n-p BJTs to supply the first and second current inputs, respectively.

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(71) Applicant *(for all designated States except US)*: **STMICROELECTRONICS ASIA PACIFC PTE LTD** [SG/SG], 28 Ang Mo Kio Industrial Park 2, Singapore 569508 (SG)

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **RAVISHANKER, Krishnamoorthy** [IN/SG], Blk 244 Lor Chuan, #19-05 Chuan Park, Singapore 556745 (SG)

(74) Agent: **DONALDSON & BURKINSHAW**; P.O Box 3667, Singapore 905667 (SG).

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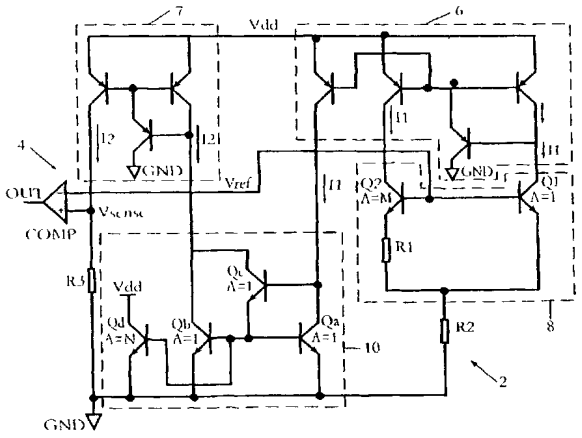
(54) Title: A THERMAL SENSOR CIRCUIT



(57) Abstract: The present invention provides a thermal sensor circuit for sensing the temperature of an integrated circuit chip, the thermal sensor circuit including: an output comparator for comparing a reference voltage, V_{ref}, with a sensed voltage, V_{sense}, the sensed voltage being measured over a sensing resistor relative to the ground potential of the circuit, a first circuit to which a reference voltage line in connected to measure V_{ref}; a first current mirror providing a first current input to the first circuit and to a compensation circuit; and second current mirror providing a second current input to the compensation circuit and to the sensing resistor. The compensation circuit provides a current gain, defined as the ratio of the second current input to the first current input, for compensating for variations in V_{ref} due to variations of the characteristics of the thermal sensing circuit arising from a manufacturing process of an integrated circuit chip on which the thermal sensor circuit is made by adjusting the second current input in dependence on the variations of the characteristics to thereby vary V_{sense} along with V_{ref}.

WO 02/08708 A1

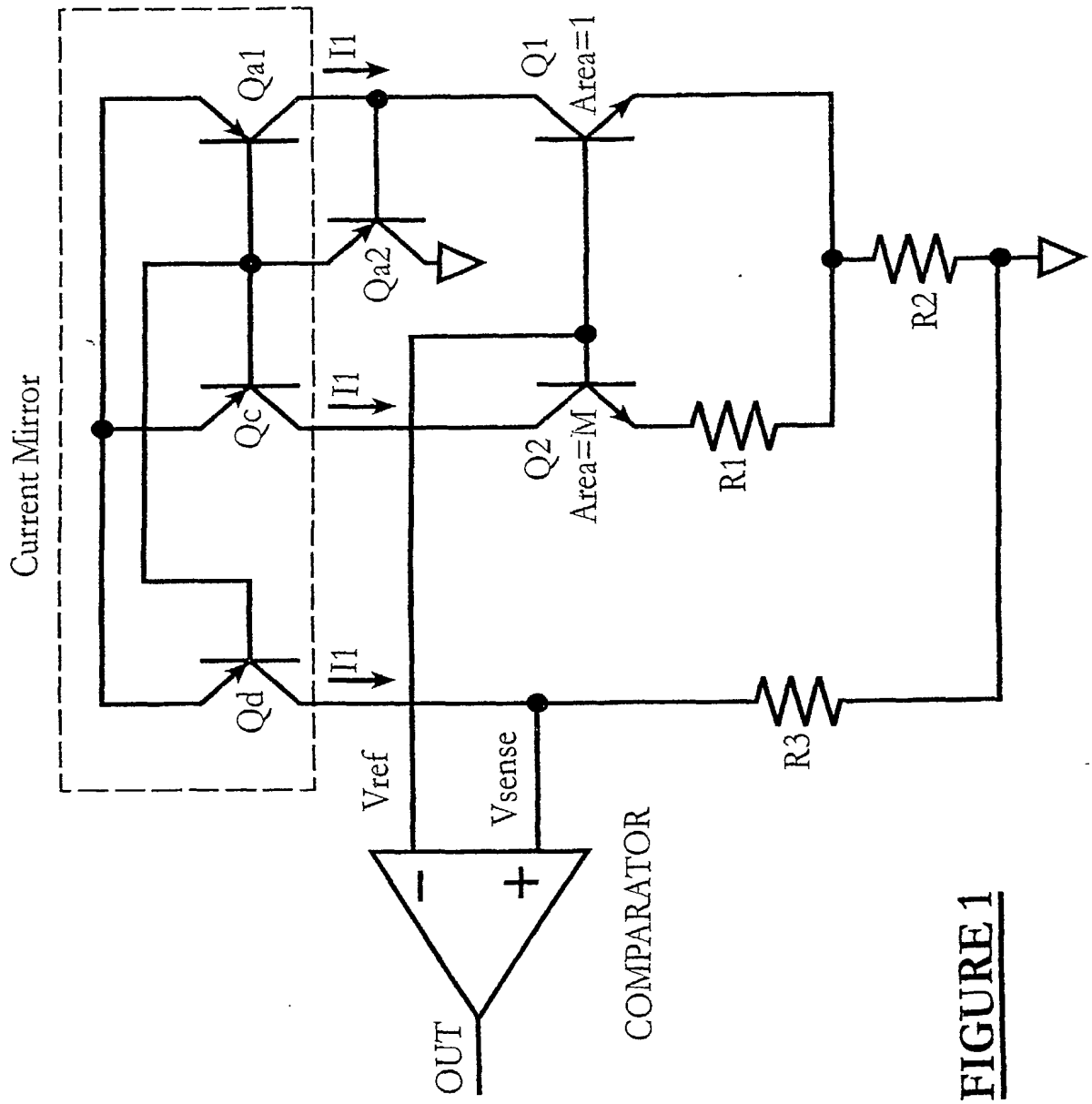

Current Mirror
Qa1
Qa2
Qc
Qd
I1
I1
I1
Q1
Area=1
Q2
Area=M
R1
R2
R3
Vref
Vsense
COMPARATOR
OUT
-
+

FIGURE 1

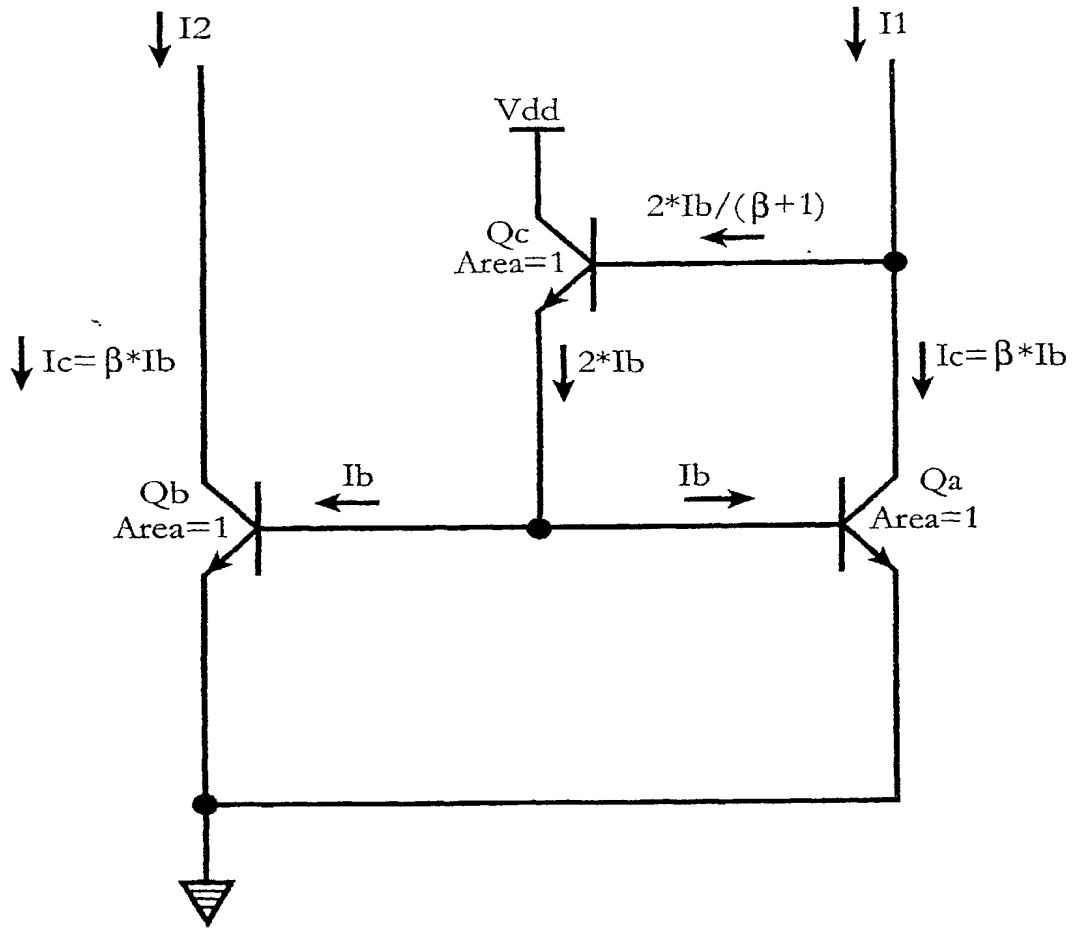

I2
I1
Vdd
2*Ib/(β+1)
Qc
Area=1
Ic=β*Ib
2*Ib
Ic=β*Ib
Ib
Ib
Qb
Area=1
Qa
Area=1

FIGURE 2

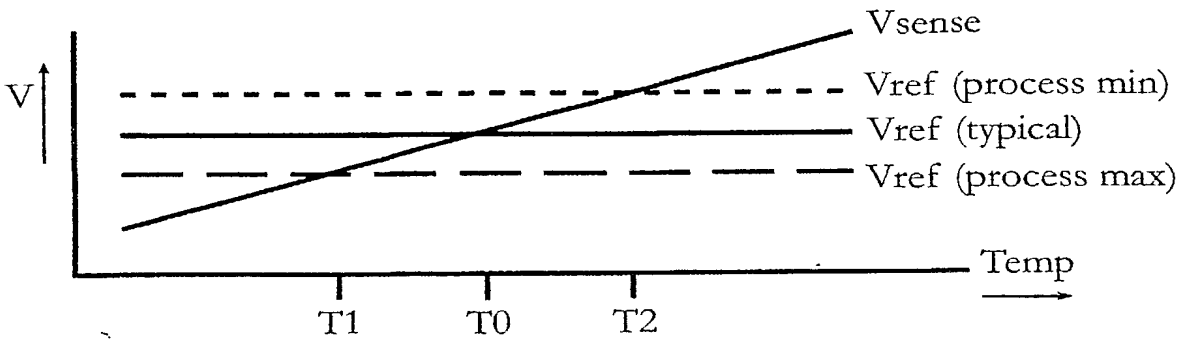


FIGURE 3A

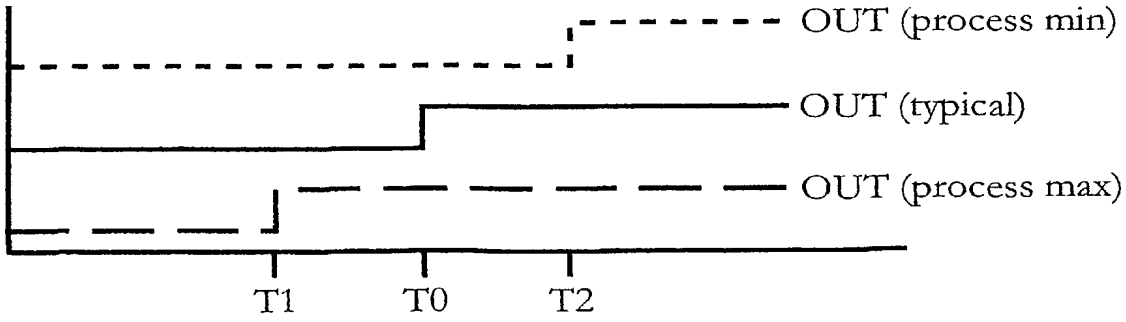


FIGURE 3B

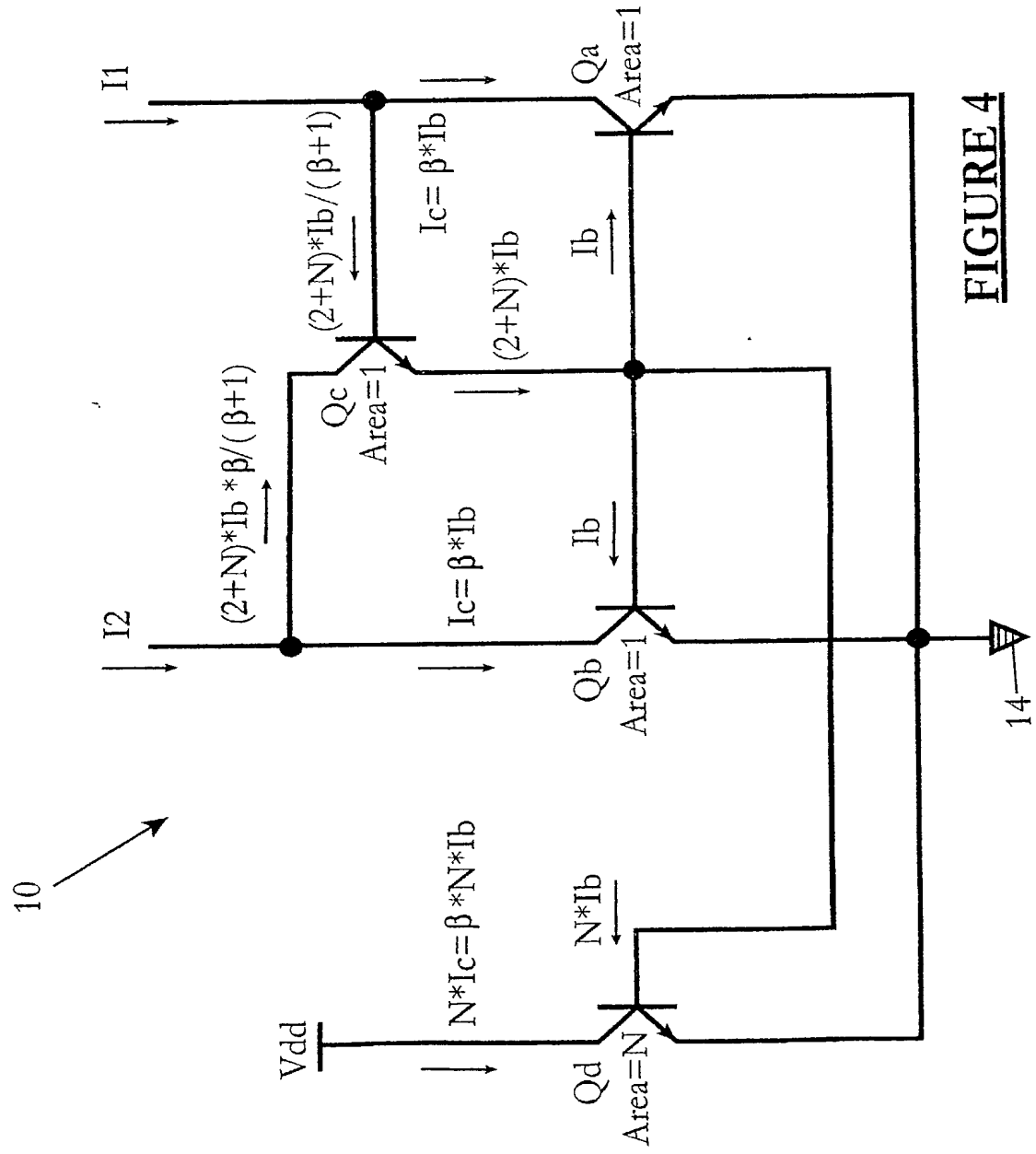

I1
I2
Vdd
Qa
Area=1
Qb
Area=1
Qc
Area=1
Qd
Area=N
Ic= β*Ib
Ib
(2+N)*Ib/(β+1)
(2+N)*Ib
(2+N)*Ib *β/(β+1)
N*Ic=β *N*Ib
N*Ib
10
14

FIGURE 4

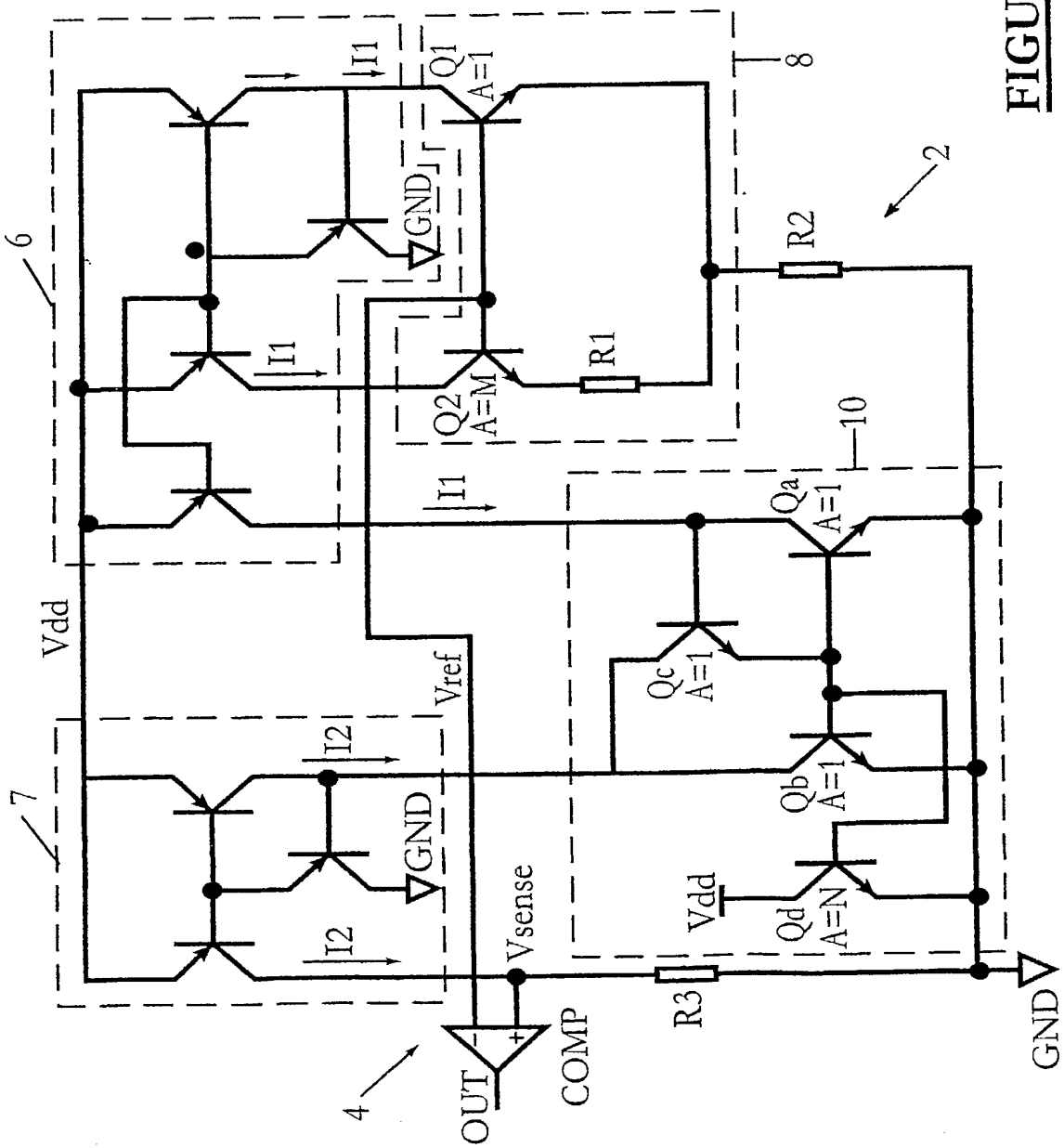

I1
Q1
A=1
GND
8
2
6
R2
I1
R1
Q2
A=M
10
I1
Qa
A=1
Vdd
Qc
A=1
Vref
I2
7
GND
Qb
A=1
Vsense
Vdd
Qd
A=N
I2
R3
GND
4
OUT
COMP

FIGURE 5

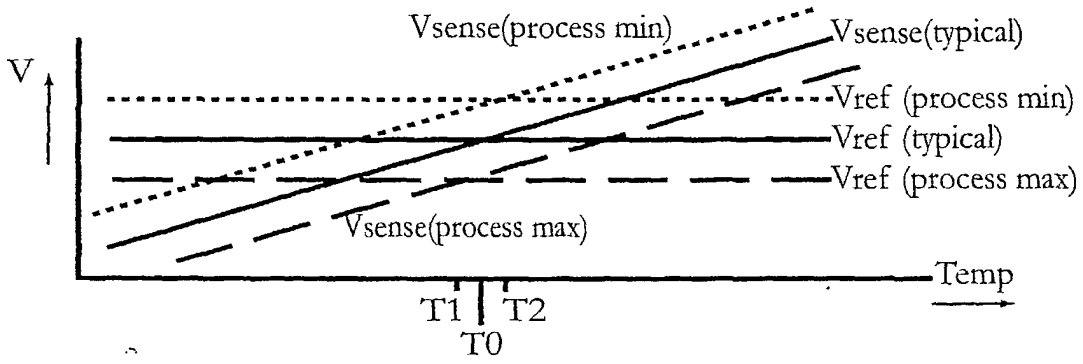


FIGURE 6A

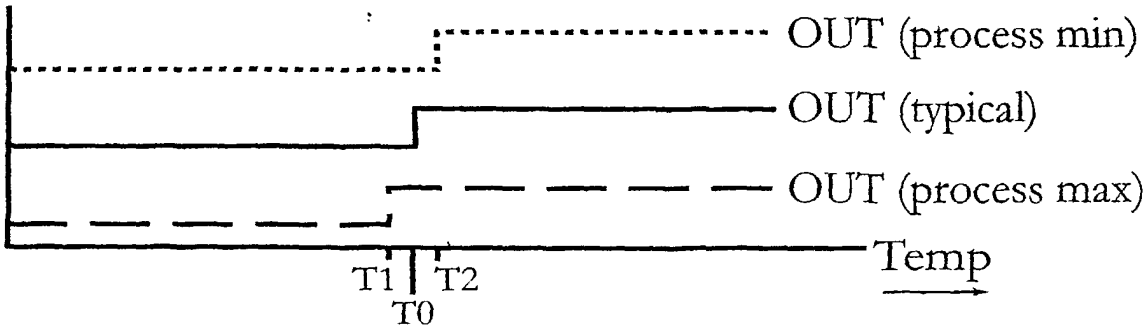


FIGURE 6B

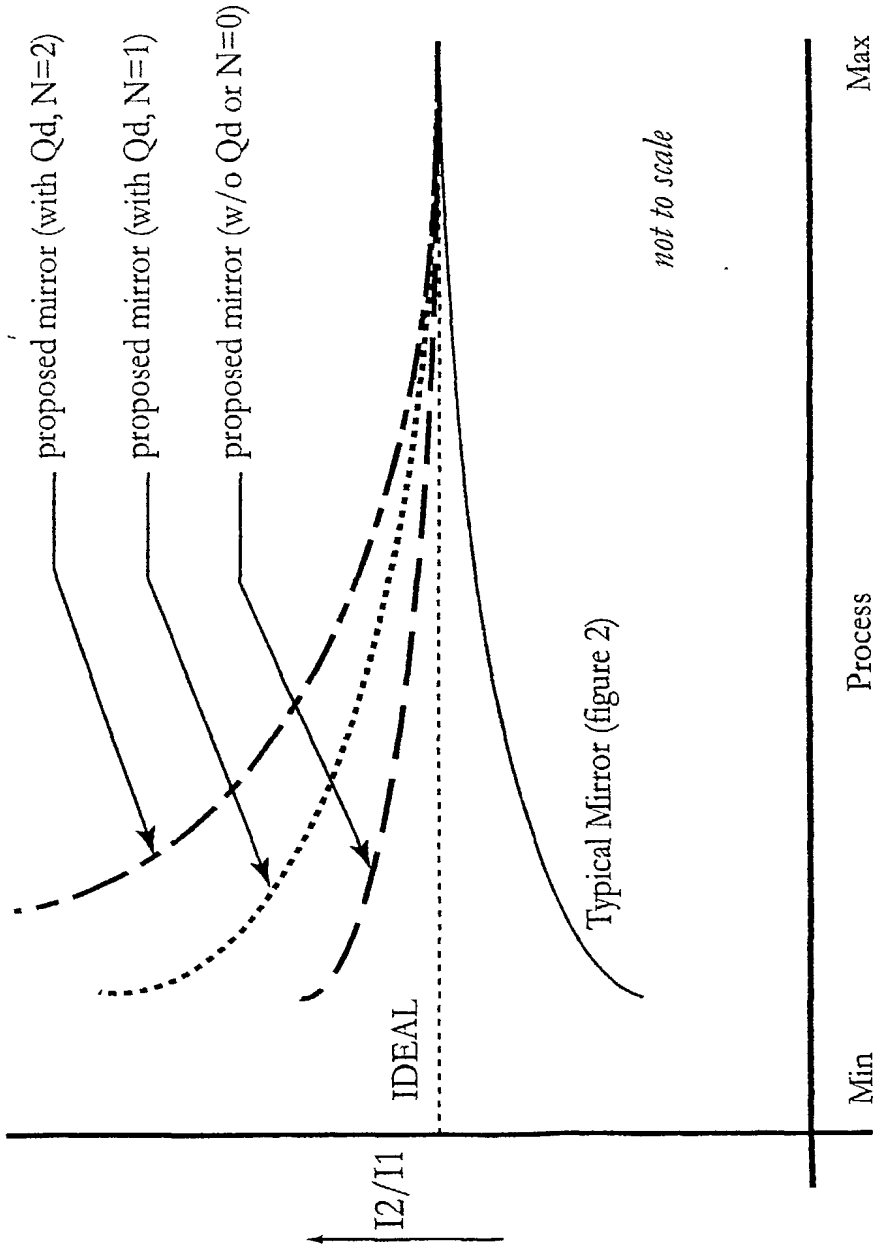

proposed mirror (with Qd, N=2)
proposed mirror (with Qd, N=1)
proposed mirror (w/o Qd or N=0)
not to scale
Typical Mirror (figure 2)
IDEAL
I2/I1
Min
Process
Max

FIGURE 7

EXPRESS MAIL NO. EV064844968US

Please type a plus sign (+) inside this box [+]

PTO/SB/01 (10-01) (modified)

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		
	Attorney Docket No	851663.433USPC
	First Named Inventor	Krishnamoorthy Ravishanker
	COMPLETE IF KNOWN	
	Application Number	10/088,976
	Filing Date	March 26, 2002
	Group Art Unit	Not yet known
	Examiner's Name	Not yet known

[ ] Declaration Submitted with Initial Filing [X] Declaration Submitted after Initial Filing

As the below named inventor(s), I/we hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A THERMAL SENSOR CIRCUIT

(Title of Invention)

the specification of which was filed on (MM/DD/YYYY) **July 26, 2000**

the specification of which is attached hereto [ ]

as United States Application Number or PCT International Application Number **PCT/SG00/00108**

Express Mail No

and was amended on (MM/DD/YYYY) *(if applicable)*

I/we have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

In addition, I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including material information which became available between the filing date of the prior application and the National or PCT International filing date of the continuation-in-part application, if applicable.

I/we hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Claimed	Certified Copy Attached? YES	NO
PCT/SG00/00108	WO	July 26, 2000	Y		X

Additional foreign application numbers are not listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I/we hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application No.	Filing Date (MM/DD/YYYY)	Application No.	Filing Date (MM/DD/YY)

Additional provisional application numbers are not listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

1-00

Direct all communications to Customer Number **00500**

Name	Robert Iannucci	of SEED INTELLECTUAL PROPERTY LAW GROUP PLLC					
Address	701 Fifth Avenue, Suite 6300						
City	Seattle WA		*State*	WA	*Zip*	98104-7092	
Country	U.S.A.	*Telephone*	(206) 622-4900	*Fax*	(206) 682-6031		

I/~~we~~ hereby declare that all statements made herein of my/~~our~~ own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

2-01

Sole or First Inventor:	**Krishnamoorthy Ravishanker**						
Given Name (first and middle [if any])			Family Name or Surname				
Krishnamoorthy			**Ravishanker**				
Inventor's Signature X		SGX			Date X	29-APRIL-02	
Residence: City	**Singapore**	State	**Singapore**	Country	**SG**	Citizenship	**IN**
Post Office Address	**Blk 244 Lor. Chuan, #19-05, Chuan Park**						
City	**Singapore**	State	**SG**	Country	**SG**		

Additional Inventor:							
Given Name (first and middle [if any])			Family Name or Surname				
Inventor's Signature					Date		
Residence: City		State		Country		Citizenship	
Post Office Address							
City		State		Country			

Additional Inventor:							
Given Name (first and middle [if any])			Family Name or Surname				
Inventor's Signature					Date		
Residence. City		State		Country		Citizenship	
Post Office Address							
City		State		Country			

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